DESIGN AND PERFORMANCE OF A FREQUENCY DIVIDE — MULTIPLY CASCADE FOR TRANSPONDER APPLICATIONS

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ABSTRACT

The design of an S-band varactor frequency doubler and a divide-by-two circuit is presented. The experimental response of the divider and multiplier in cascade to a CW FM signal and to a bi-phase modulated signal are given. The distortion introduced by the cascade for a FM signal is only seven percent and is negligible for the bi-phase modulated signal.

INTRODUCTION

This paper briefly describes the design and performance of a varactor frequency divider and a frequency multiplier connected in cascade. A divider-amplifier-multiplier cascade has the potential for high efficiency solid state transponders and eliminates the need for conventional high-power, high-efficiency up converters. Figure 1 shows the block diagram of a possible X-band transponder. This design approach has applications to communication satellites, remotely piloted vehicles, or to expendable jammers in electronic counter measures (ECM).

FREQUENCY DOUBLER AND DIVIDE-BY-TWO CIRCUITS

Two nearly identical circuits were designed and fabricated; one for the divide-by-two circuit and one for the frequency doubler. These circuits are distributive circuit realizations of the stable frequency multiplier design suggested by Grayzel.[1] Each circuit consists of two diplexers each composed of a complimentary bandpass and bandstop filter pair. The complimentary filter pair presents a constant real impedance to the diode at all frequencies. A matching network is inserted between the diode and the common port of the filter pair to match the diode at both the input and output frequency.

Two identical coaxial line models of the circuit were fabricated; one to be used as a frequency multiplier from 1.7 to 3.4 GHz and the second as a frequency divider from 3.4 GHz to 1.7 GHz.[2] Figure 2 is a photograph of the frequency divider with the top split half removed to show the center conductors. The input and output ports and the common port of the diplexers are 50 ohms. A tapered line was used to transform the 50 ohms to the real part of the diode impedance of 19 ohms. A matching network consisting of two series stubs (one with a pole at the third harmonic) was designed to resonate the diode at the fundamental and second harmonic. The measured performance of the circuits is summarized in Table 1.

RESPONSE TO CW FM SIGNAL

Individually and in cascade the multiplier and the divider circuits were subjected to a CW FM signal with a maximum modulation frequency of 10 MHz and a modulation index of $(\Delta f/fm) = 10$. FM discriminators at 1.7 GHz and 3.4 GHz were fabricated. The measured average distortion over a 100 MHz bandwidth of the modulator and discriminator were 2.1% and 2.4% at 1.7 GHz and 3.4 GHz respectively.* The average distortion of the frequency doubler for a CW FM signal measured over a 100 MHz bandwidth was 5%. The symmetry of the input spectrum was preserved in the output spectrum, but the bandwidth of the output was double the bandwidth of the input as predicted from theory. Figure 3 shows the input spectrum and the output spectrum of the frequency divide-by-two circuit when subjected to a CW FM signal. Note that as a divider the symmetry of the spectrum is preserved and the contraction of the output spectrum is as expected. The measured distortion as a divider was 6%.

Table 1

Performance of Experimental S-Band Varactor Frequency Doubler and Divide-by-Two Circuits to a CW Signal

Parameter	Multiplier	Divider
Input Frequency	1.7 GHz	3.4 GHz
Input Power	1.0 Watt	1.1 Watt
Output Power	0.63 Watt	0.704 Watt
Input VSWR	1.40	1.45
3-dB Bandwidth	260 MHz	210 MHz
Bias Voltage	-10.9 Volts	-9.0 Volts
Harmonic Level	-50 dB	-30 dB

With the frequency doubler and the divider connected in cascade, a CW FM signal with a carrier frequency of 3.4 GHz was fed into the divider and the corresponding signal at 3.4 GHz was measured at the multiplier output. The measured average distortion of the cascade was 7.3% over a 100 MHz bandwidth. The measured value of 7.3% includes the distortion introduced by the modulator and discriminator. These results indicate that the divide-multiply scheme for transponders has the potential for low distortion FM systems.

RESPONSE TO A BI-PHASE MODULATED SIGNAL

Bi-phase modulated signals are used for digital communications. Experiments were conducted to examine the distortion introduced by the divide-multiply cascade on a bi-phase modulated signal. The phase of the input signal was modulated by a square wave generator

*The distortion is defined as the ratio of the root mean square of the harmonic signals of the modulating signal divided by the fundamental signal level at the output of the discriminator.

at a 100 kHz/s rate. Measurements were made of the spectrum and the demodulated waveforms of both the input signal and the output signal of the divide-multiply cascade. Figure 4 shows the demodulated waveforms of the bi-phase modulated signals at the input and output of the divide-multiply cascade. Figure 5 shows the corresponding spectrums of the input and output signals. Comparison of the input and output waveforms and spectrum show that there is little or no perceptible distortion introduced in the bi-phase modulated signal by the divide-multiply cascade. Therefore such a scheme has potential application to digital communications.

RESPONSE TO A 50 MHz JAMMING SIGNAL

A jamming signal was fed together with the input signal at 3.4 GHz into a hard limiter with a 50 MHz bandwidth and then through the divide-multiply cascade. When the jamming signal is large compared to the desired signal, envelope nulls appear in the output signal of the bandpass limiter at a maximum rate consistent with the system bandwidth. Figure 6 shows photographs of the sampling oscilloscope traces of both the input and output signal waveforms to the divide-multiply cascade. The effect of the divide-multiply circuits on the jammed signal is to increase the duration of the nulls in the output signal. This increase is a consequence of the fact that once the multiplier (divider) has been turned off (the envelope of the input signal has decreased to zero) a finite time is required to establish the divide-multiply action again.

CONCLUSIONS

The concept of a transponder that utilizes a divider-high power amplifier-multiplier chain or cascade has been presented and experimentally demonstrated to introduce low distortion to FM signals and bi-phase modulated signals. These results demonstrate the feasibility of using a divider-multiplier cascade in an all solid-state transponder which has increased efficiency over the conventional transponder using an upconverter in a less complex design.

REFERENCES

1. A.I. Grayzel and R.T. Minkoff, "A New Technique for Designing Highly Stable High Efficiency Varactor Multiplier Chains," 1969 International Microwave Symposium Digest, pp. 131-135 (May 5-7, 1969).

2. D. Parker and A.K. Gorwara, "Design of an S-Band Varactor Frequency Divider," in preparation.

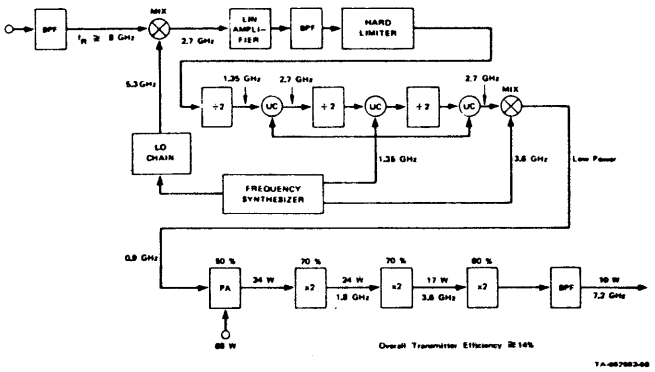


Figure 1 Proposed Solid State Repeater Block Diagram Using Frequency Dividers and Multipliers

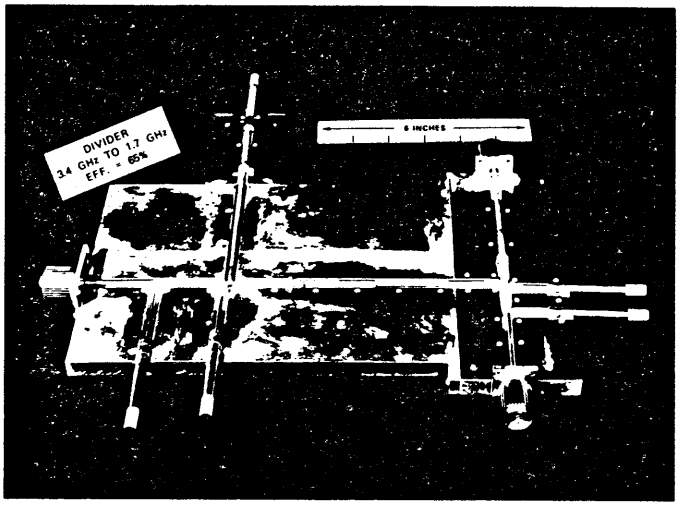


Figure 2 Photograph of Frequency Divider Circuit

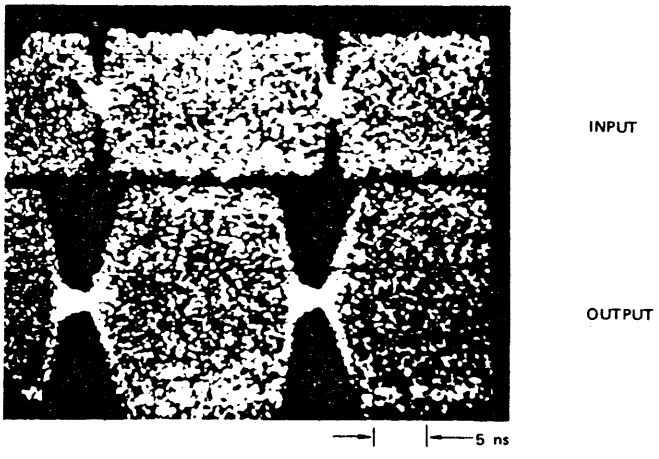
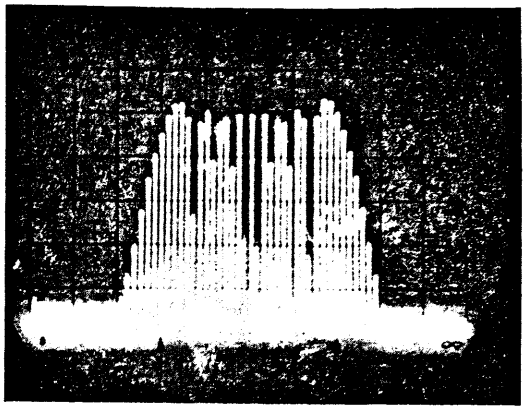
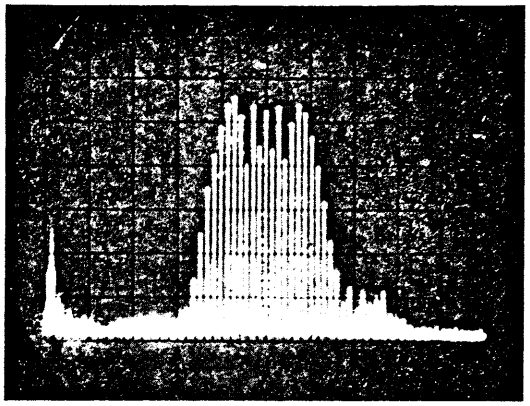


Figure 6 Input and Output Signals of Divide-Multiply Cascade Subjected to a Jamming Signal After Limiting by a Bandpass Limiter

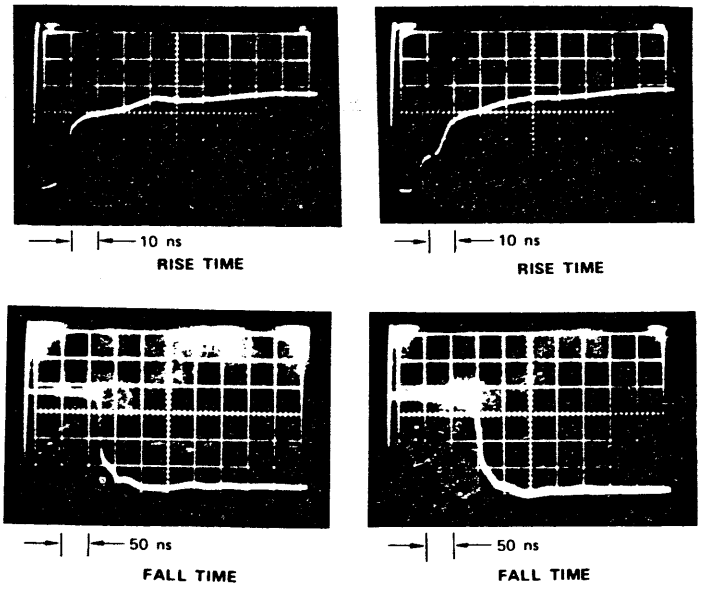


Input Center Frequency 3.4 GHz



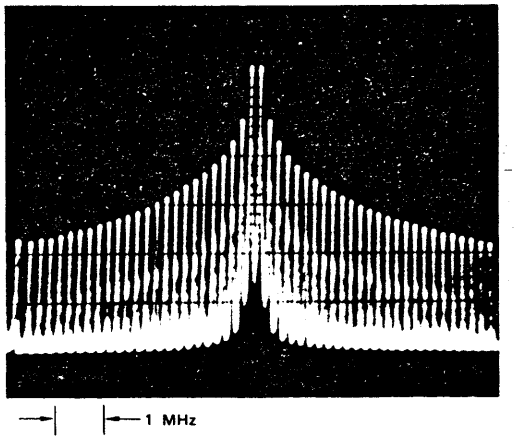
Output Center Frequency 1.7 GHz

Figure 3 Spectrums of a CW FM Signal at the Input and Output of Divide-by-Two Circuit. Horizontal scale: 30 MHz/cm. Input power = 0.63 W; Output power = 1.2 W.

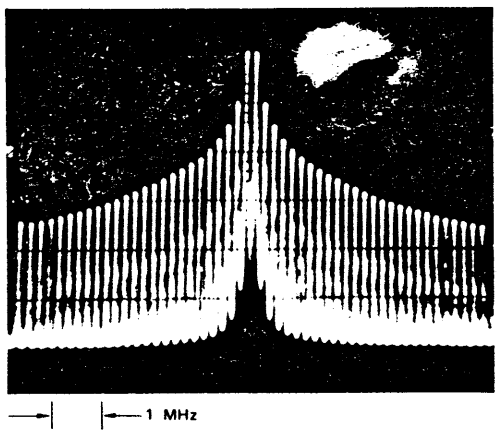


(a) Input (b) Output

Figure 4 Demodulated Waveforms of the Bi-Phase Modulated Signals at the Input and Output of Divide-Multiply Cascade



(a) Input



(b) Output

Figure 5 Spectrum of Bi-Phase Modulated Signal at Input and Output of Divide-Multiply Cascade. Center Frequency = 3.4 GHz. IF Bandwidth = 10 kHz.